ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	SEGMENTED ALGORITHMIC PATTERN GENERATOR

Application Number :

Confirmation Number:

First Named Applicant: Amy Gottsche

Attorney Docket Number: BUR920030165US1

Art Unit:

Examiner:

Search string: (5872797 or 6044480 or 6314540 or 5862149 or 6615380 or 5802075 or 5097468 or 5430736 or 5010552 or 4994732 or 6212667 or 6092225).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5872797	1999-02-16	Theodoseau			
	2	6044480	2000-03-28	Keen			
	3	6314540	2001-11-06	Huott et al.			
	4	5862149	1999-01-19	Carpenter et al.			
	5	6615380	2003-09-02	Kapur et al.			
	6	5802075	1998-09-01	Carpenter et al.			
	7	5097468	1992-03-17	Earlie			
	8	5430736	1995-07-04	Takeoka et al.			
	9	5010552	1991-04-23	Dias et al.			
	10	4994732	1991-02-19	Jeffrey et al.			
	11	6212667	2001-04-03	Geer et al.			
	12	6092225	2000-07-18	Gruodis et al.			

Signature

Examiner Name	Date
John J. Tabone Jr	9/8/05

Supplemental Form PTO-1449 (Modified)	Attorney Docket No.: BUR920030165US1	Serial No: 10/710802
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: Amy J. Gottsche, et al.	
(Use several sheets if necessary) Page 1 of 1	Filing Date: 08/04/04	Group: Unassigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
DJP		2-24584	01-26-1990	Japan			☒ Abstract	☐
DJP		2001-349930	12-21-2001	Japan			☒ Abstract	☐
							☐	☐
							☐	☐
							☐	☐

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

DJP		C.W. Cha, et al., "Array Test Pattern Generation Algorithms for a Per Pin Tester", IBM Technical Disclosure Bulletin, Vol. 30, No. 10, March 1988.
DJP		J.T. Muhr, et al., "Test Pattern Generation for Partitioned Programmable Logic Arrays", IBM Technical Disclosure Bulletin, Vol. 26, No. 3B, August 1983.
V		P.Y.W. Au, et al., "Technique for VLSI In-Circuit Testing", IBM Technical Disclosure Bulletin, Vol. 31, No. 4, September 1988.

EXAMINER John J. Tabone Jr. DATE CONSIDERED 9/8/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.